# Lab #4: SPICE Netlist Simulation

Acknowledgement: This lab assignment is created based on Professor Hajimorad’s lab assignments from EENG 331 - Spring 2015 quarter.

Lab type: Self. Complete the lab tasks on your own.

Lab objectives: The objective of this lab is to perform SPICE netlist simulation using LTspice to determine the transistor operating point parameter values.

## Pre-lab

Calculate the values of µnCox and µpCox. Where Cox can be computed as ϵox / tox

Given µn = 400cm2/V.s, µp = 200cm2/V.s, ϵox = 3.9ϵo, ϵo = 8.854E-14F/cm, tox = 6.903nm.

**You must show the prelab results (i.e., solution by hand in clear writing) to your instructor when asked. Failure to do so will result in poor lab grade.**

## Part#1: SPICE Netlist Simulation

Use “Notepad” or similar text file editor and create an empty file called “Lab3.net”. Make sure you save it correctly, so it is not “Lab3.net.txt”.

Open the LTspice program which should be installed on all the lab computers and is free to install on your home system. Then complete the following tasks.

* Select File\Open
* Ensure the “Files of type:” is set to “Netlists (\*.cir; \*.net; \*.sp)”
* Navigate to your “Lab3.net” file directory and open the file.

Now carefully enter the contents shown in Figure 1 into your Lab3.net file and save the file. (You may simply copy and paste the contents to save time)

This is my first SPICE netlist in EENG 331

V1 1 0 DC 1.8

V2 2 0 DC 1.8

V3 3 0 DC 0

V4 4 0 DC 0

X1 1 2 3 4 nmos\_ee331 width=10u length=1u

X2 4 3 2 1 pmos\_ee331 width=10u length=1u

.SUBCKT nmos\_ee331 d g s b width=10u length=1u

M1 d g s b nmos\_internal W='width' L='length'

+ AD='width\*2e-6' AS='width\*2e-6' PD='4e-6+width' PS='4e-6+width'

.MODEL nmos\_internal NMOS LEVEL=1 uo=400 vto=0.4 lambda=0

+ tox=6.903n gamma=1 phi=0.6 cgdo=0.5n cgso=0.5n cj=0.001 mj=0.5 pb=1

+ cjsw=0.1n mjsw=0.5 capop=0

.ENDS

.SUBCKT pmos\_ee331 d g s b width=10u length=1u

M2 d g s b pmos\_internal W='width' L='length'

+AD='width\*2e-6' AS='width\*2e-6' PD='4e-6+width' PS='4e-6+width'

.MODEL pmos\_internal PMOS LEVEL=1 uo=200 vto=-0.4 lambda=0

+ tox=6.903n gamma=1 phi=0.6 cgdo=0.5n cgso=0.5n cj=0.001 mj=0.5 pb=1

+ cjsw=0.1n mjsw=0.5 capop=0

.ENDS

.OP

.END

Figure 1

**NOTE** the following:

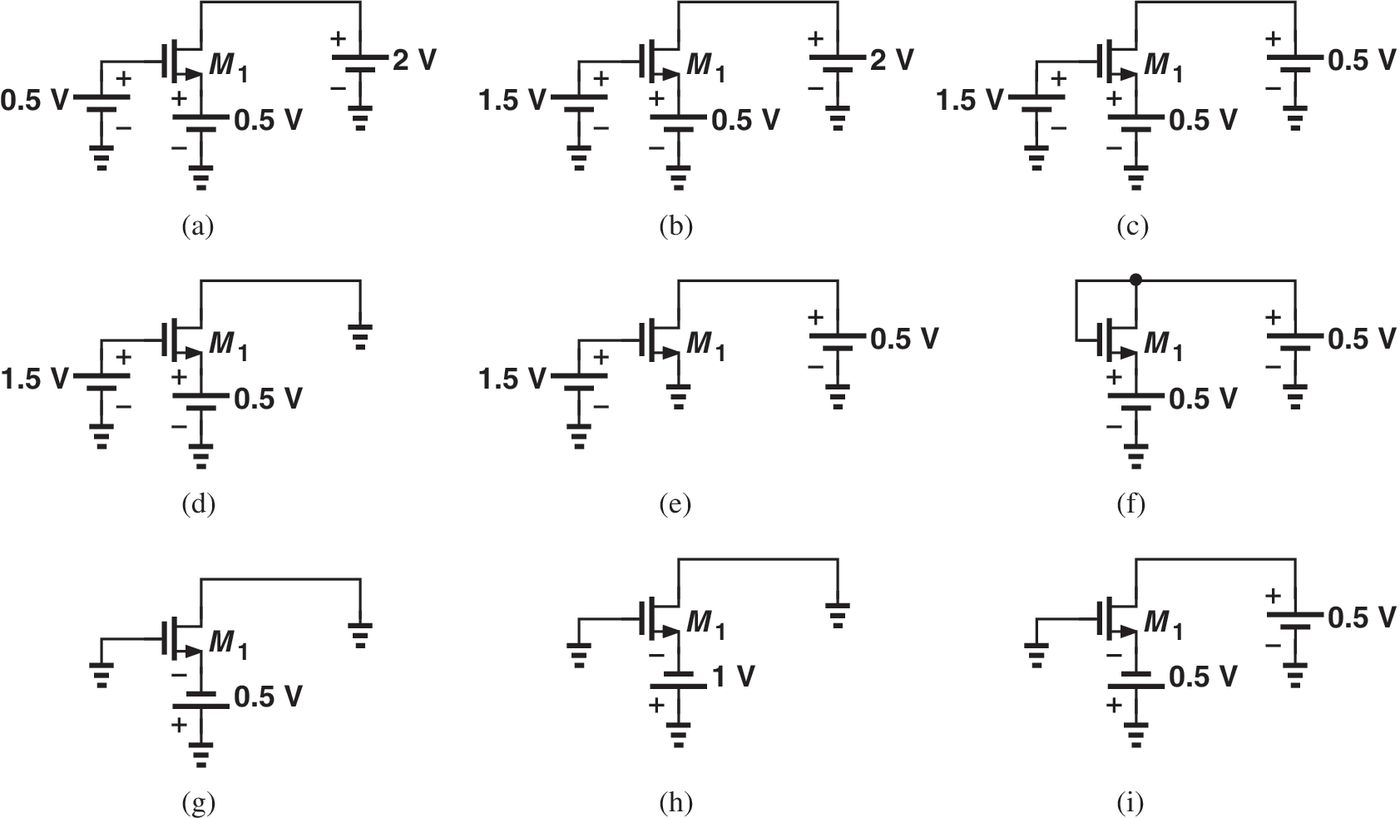
* The first line of a netlist is **ALWAYS** treated as a comment line and ignored by SPICE
* If any other line is meant to be treated as a comment, it MUST begin with an asterisk ( \* )
* Four voltage sources have been defined in the netlist. One connected between node 1 and ground (named V1), another connected between node 2 and ground (named V2), another connected between node 3 and ground (named V3), and another connected between node 4 and ground (named V4)
* Two MOS transistors have been defined in the netlist. One is named X1, while the other is named X2. In this course, we are using SPICE’s “subcircuit” feature to utilize MOSFETs with the appropriate device parameters. As a result, a MOSFET’s name (irrespective of whether it is a NMOS or PMOS) **MUST** begin with the letter X.
* Note the following order for MOSFET node definitions in SPICE: the first specified node is the drain, second specified node is the gate, third specified node is the source, and the fourth specified node is the bulk (i.e. body). The same order applies to PMOS transistors.
* “nmos\_ee331” comes after the MOSFET nodes in Figure 3 because that is the subcircuit name used for the NMOS transistor in EE331. For PMOS transistors, the “pmos\_ee331” subcircuit name has been used
* Each of the MOSFET declaration lines end with the width and length of the transistor being specified
* The two .SUBCKT->.ENDS lines in the netlist define the NMOS and PMOS subcircuits
* The .OP statement in the netlist instructs SPICE to perform an “operating point” analysis. This essentially computes all of the DC voltages and currents in the circuit, in addition to the small-signal parameters of all of the circuit transistors
* Finally, every netlist **MUST** end with the line .END

1. After saving your netlist file, run the SPICE simulation by clicking on the Run Icon , hitting <CTRL+R>, or via the menu: Simulate\Run.
2. Hand Calculations: Based on the netlist in Figure 1, what are the regions of operation for transistors X1 and X2? Also, calculate the drain current ID and gm for each. You may use the results from pre-lab.
3. Now, open the “SPICE Error log” file via View->SPICE Error log or press “CTRL+L” and verify your earlier hand calculations regarding transistor regions of operation, drain current and gm values.
4. From the .OP results what does vdsat represent?
5. Show your hand calculations and simulation results to the instructor
6. Using the PDF documents in Lab 3 folder, give a brief definition for each parameter in the .model netlist line.
7. Discuss the difference between level 1,2 and 3 simulation (Use the enclosed PDFs)

**Part#2: More SPICE Simulations**

1. Next, modify your netlist to simulate the circuits below. Use the same SPICE models from Part#1. Try to have a single netlist file to test all the circuits at once. Record *ID and gm* of each transistor from the SPICE netlist simulation.
2. Verify SPICE results with your hand calculations. Also, determine the region of operation for the transistor in each circuit.

***NMOS Circuits***:



***PMOS Circuits:***

